METHOD FOR MANUFACTURING AND STRUCTURE FOR TRANSISTORS WITH REDUCED GATE TO CONTACT SPACING

ABSTRACT OF THE DISCLOSURE

A method for manufacturing a transistor includes providing a transistor assembly having a semiconductor layer with a first surface, a dielectric layer disposed on the first surface, a gate electrode disposed on the dielectric layer, an insulation layer adjacent at least part of the gate electrode, and a nitride spacer layer adjacent at least part of the insulation layer. The method also includes depositing, on part of the first surface, a material that will react with the semiconductor layer to form silicide and removing the unreacted material. The method further includes etching the nitride spacer layer, depositing a pre-metal spacer layer adjacent at least part of the nitride spacer layer and at least part of the first surface, etch removing a portion of the pre-metal spacer layer to expose part of the silicided portion of the first surface, and forming a contact with the silicided portion of the first surface.